MachXO2 Breakout Board Evaluation Kit

Evaluation Board User Guide

FPGA-EB-02051-2.3

February 2022

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
DIP	Dual In-line Package
FPGA	Field-Programmable Gate Array
LED	Light Emitting Diode
LUT	Look-Up Table
NVCM	Non Volatile Configuration Memory
PCB	Printed Circuit Board
RoHS	Restriction of Hazardous Substances Directive
USB	Universal Serial Bus
WDT	Watchdog Timer

1. Introduction

This user guide describes how to start using the MachXO2™ Breakout Board, an easy-to-use platform for evaluating and designing with the MachXO2 ultra-low density FPGA. Along with the board and accessories, this kit includes a pre-loaded demonstration design. You may also reprogram the on-board MachXO2 device to review your own custom designs.

The MachXO2 Breakout Board currently features the MachXO2-7000HE device. A previous version of this board featured the MachXO2-1200ZE. The board design and features have not changed, and consequently, this document can be used as a guide for either version of the board. If you require a board featuring the MachXO2-1200ZE, Lattice recommends the MachXO2 Pico Development Kit.

See the Ordering Information section for more information.

Note: Static electricity can severely shorten the lifespan of electronic components. See the Storage Handling section of this document for handling and storage tips.

2. Features

The MachXO2 Breakout Board Evaluation Kit includes:

- MachXO2Breakout Board – The board is a 3 inches x 3 inches form factor that features the following on-board components and circuits:
  - MachXO2 FPGA – Current board version: LCMXO2-7000HE-4TG144C
    (Previous board version no longer available: LCMXO2-1200ZE-1TG144C)
  - USB mini-B connector for power and programming
  - Eight LEDs
  - 60-hole prototype area
  - Four 2 x 20 expansion header landings for general I/O, JTAG, and external power
  - 1 x 8 expansion header landing for JTAG
  - 3.3 V and 1.2 V supply rails
- Pre-loaded Demo – The kit includes a pre-loaded counter design that highlights use of the embedded MachXO2 oscillator and programmable I/O configured for LED drive.
- USB Connector Cable – The board is powered from the USB mini-B socket when connected to a host PC. The USB channel also provides a programming interface to the MachXO2 JTAG port.
- Lattice Breakout Board Evaluation Kits Web Page – Visit www.latticesemi.com/breakoutboards for the latest documentation (including this guide) and drivers for the kit.

The content of this user guide includes demo operation, programming instructions, top-level functional descriptions of the Breakout Board, descriptions of the on-board connectors, and a complete set of schematics

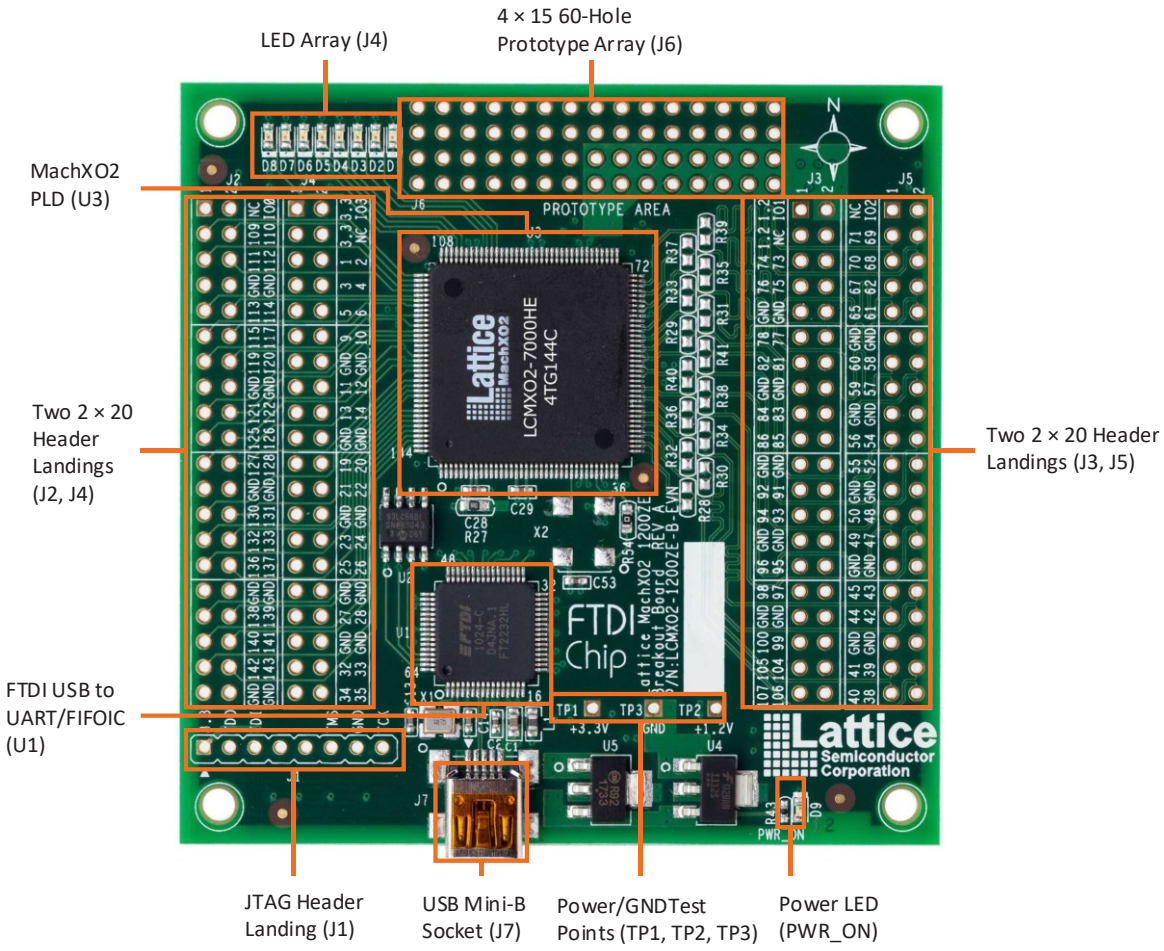


Figure 2.1. MachXO2 Breakout Board, Top Side

3. Storage Handling

Static electricity can shorten the lifespan of electronic components. Observe these tips to prevent damage that could occur from electro-static discharge:

- Use anti-static precautions such as operating on an anti-static mat and wearing an anti-static wrist-band.
- Store the evaluation board in the packaging provided.
- Touch a metal USB housing to equalize voltage potential between you and the board.

4. Software Requirements

You should install the following software before you begin developing designs for the Breakout Board:

- Lattice Diamond® design software
- FTDI Chip USB hardware drivers (installed as an option within the Diamond installation program)

5. MachXO2 Device

This board currently features the MachXO2-7000HE FPGA which offers embedded Flash technology for instant-on, non-volatile operation in a single chip. Numerous system functions are included, such as two PLLs and 256 Kbits of embedded RAM plus hardened implementations of I2C, SPI, timer/counter, and user Flash memory. Flexible, high performance I/O support numerous single-ended and differential standards including LVDS, and also source synchronous interfaces to DDR/DDR2/LPDDR DRAM memory. The 144-pin TQFP package provides up to 114 user I/O in a 20 mm × 20 mm form factor. Previous versions of this board featured the MachXO2-1200ZE PLD in the same package. This version of the board is no longer available. A complete description of this device can be found in the MachXO2 Family Data Sheet (FPGA-DS-02056).

6. Demonstration Design

Lattice provides a simple, pre-programmed demo to illustrate basic operation of the MachXO2 device. The design integrates an up-counter with the on-chip oscillator.

Note: You may obtain your Breakout Board after it has been reprogrammed. To restore the factory default demo and program it with other Lattice-supplied examples see the Download Demo Designs section.

6.1. Run the Demonstration Design

Upon power-up, the preprogrammed demonstration design automatically loads and drives the LED array in an alternating pattern. The program shows a clock generator based on the MachXO2 on-chip oscillator. The counter module is clocked at the oscillator default frequency of 2.08 MHz to illustrate how low speed timer functions can be implemented with a FPGA. The 22-bit up-counter further divides the clock to advance the LED display approximately every 500 ms. The resulting light pattern appears as an alternating pair of lit LEDs per row.

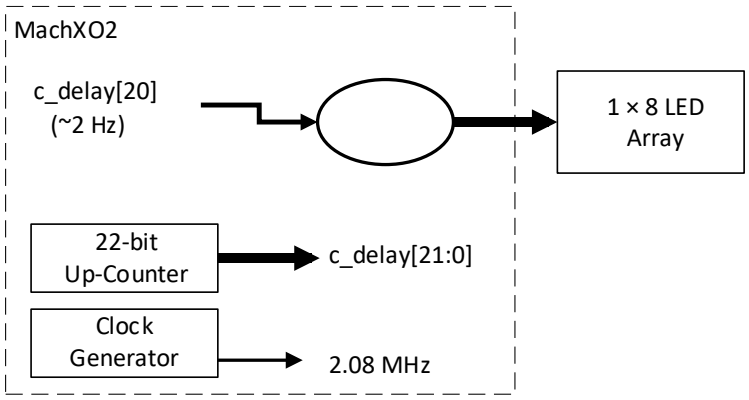


Figure 6.1. Demonstration Design Block Diagram

WARNING: Do not connect the Breakout Board to your PC before you follow the driver installation procedure of this section.

Communication with the Breakout Board with a PC via the USB connection cable requires installation of the FTDI chip USB hardware drivers. Loading these drivers enables the computer to recognize and program the Breakout Board. Drivers can be loaded as part of the installation of Lattice Diamond design software or Diamond Programmer, or as a standalone package.

To load the FTDI Chip USB hardware drivers as part of the Lattice Diamond installation:

1. Select **Programmer Drivers** in the Product Options of Lattice Diamond Setup.
2. Select **FTDI Windows USB Driver** or **All Drivers** in the LSC Drivers Install/Uninstall dialog box.
3. Click **Finish** to install the USB driver.
4. After the driver installation is complete, connect the USB cable from a USB port on your PC to the board's USB mini-B socket (J2). After the connection is made, a blue Power LED (D1) lights indicating the board is powered on.
5. The demonstration design automatically loads and drive the LED array in a repeating pattern.

To load the FTDI chip USB hardware drivers via the stand-alone package on a Windows system:

1. Download the FTDI Chip USB Hardware Drivers package from the Lattice website.
2. Extract the FTDI chip USB Hardware driver package to your PC hard drive.
3. Connect the USB cable from a USB port on your PC to the board's USB mini-B socket (J2). After the connection is made, a blue Power LED (D1) lights indicating the board is powered on.

4. If you are prompted, *Windows may connect to Windows Update* select **No, not this time** from available options and click Next to proceed with the installation. Choose the **Install from specific location (Advanced)** option and click **Next**.
5. Search for the best driver in these locations and click the **Browse** button to browse to the Windows driver folder created in the Download Windows USB Hardware Drivers section. Select the **CDM 2.04.06 WHQL Certified** folder and click **OK**.
6. Click **Next**. A screen displays as Windows copies the required driver files. Windows display a message indicating that the installation was successful.
7. Click **Finish** to install the USB driver.
8. The demonstration design automatically loads and drive the LED array in a repeating pattern.

See the Troubleshooting section of this guide if the board does not function as expected.

6.2. Download Demo Designs

The counter demo is preprogrammed into the Breakout Board, however over time it is likely your board will be modified. Lattice distributes source and programming files for demonstration designs compatible with the Breakout Board. The demo design for the 1200ZE version of the board is available on the web. Use the same design files for MachXO2-7000HE. Change the device in the Diamond Software tool and re-run the process flow to generate the JEDEC for MachXO2-7000HE. The description below references the 7000HE version.

To download demo designs:

1. Browse to the Lattice Breakout Board Evaluation Kits web page (www.latticesemi.com/breakoutboards) of the Lattice web site. Select **MachXO2 Breakout Board Demo Source** and save the file.
2. Extract the contents of **MachXO21200ZEBreakoutBoardDemoDesignSource.zip** to an accessible location on your hard drive.
3. Open the Project in the Diamond Design Software and change the device to MachXO2-7000HE-4TG144C.
4. Run the Process Flow and regenerate the JEDEC file.

Continue to Programming a Demo Design with the Lattice Diamond Programmer.

6.3. Programming a Demo Design with the Lattice Diamond Programmer

The demonstration design is pre-programmed into the MachXO2/MachXO3 board by Lattice. If you have changed the design but now want to restore the board to factory settings, use the procedure described below.

To program the MachXO2 device:

1. Install, license and run Lattice Diamond software. See http://www.latticesemi.com/latticediamond for download and licensing information.
2. Connect the USB cable to the host PC and the MachXO3 board.
3. From Diamond, open the *Default_pattern_w_standby.ldf* project file.
4. Click the **Programmer** icon.
5. Click **Detect Cable**. The Programmer detects the cable (Cable: USB2, Port: FTUSB-0). If the cable is not detected, see the Troubleshooting section.
6. Click the **Program** icon. When complete, **PASS** is displayed in the Status column.

7. MachXO2 Breakout Board

This section describes the features of the MachXO2 Breakout Board in detail.

7.1. Overview

The Breakout Board is a complete development platform for the MachXO2 FPGA. The board includes a proto-typing area, a USB program/power port, an LED array, and header landings with electrical connections to most of the FPGA's programmable I/O, power, and JTAG pins. The board is powered by the PC's USB port or optionally with external power. You may create or modify the program files and reprogram the board using Lattice Diamond software.

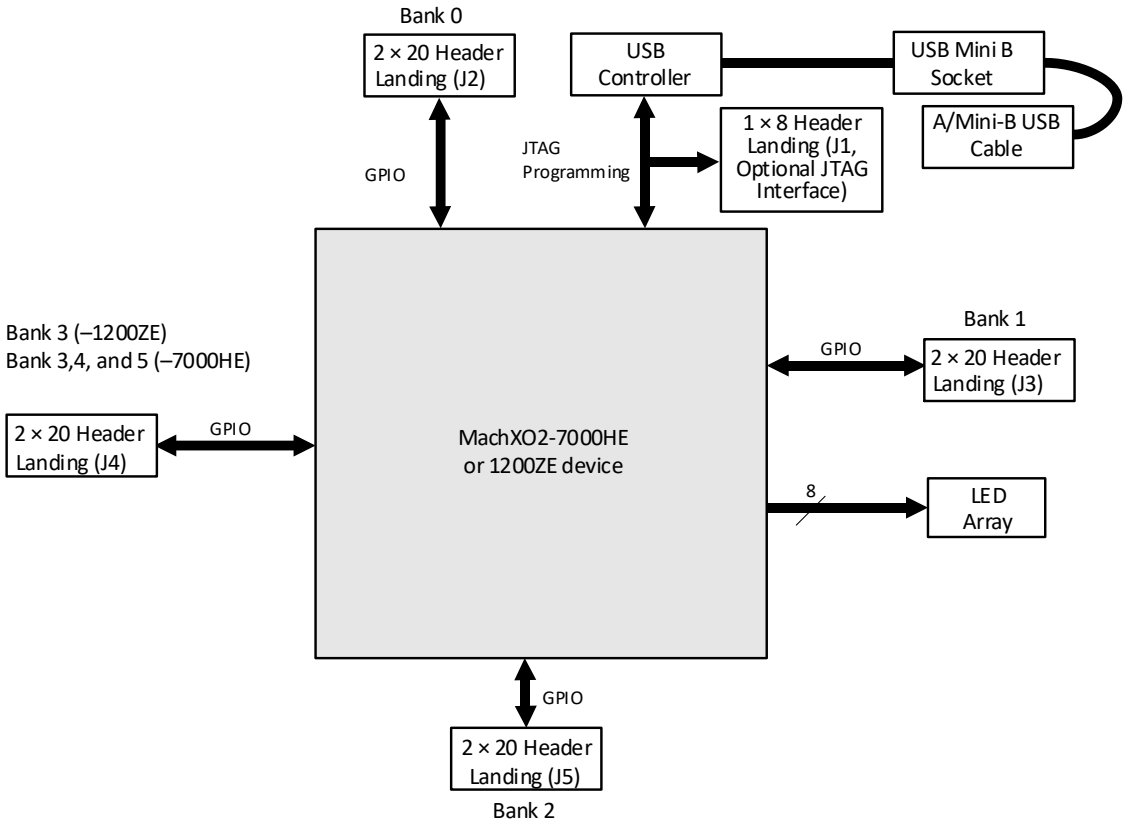


Figure 7.1. MachXO2 Breakout Board Block Diagram

Table 7.1 describes the components on the board and the interfaces it supports.

Table 7.1. Breakout Board Components and Interfaces

Component/Interface	Type	Schematic Reference	Description
Circuits			
USB Controller	Circuit	U2: FT2232H	USB-to-JTAG interface and dual USB UART/FIFO IC
USB Mini-B Socket	I/O	J7:USB_MINI_B	Programming and debug interface
Components			
LCMXO2	FPGA	U3: LCMXO2-7000HE-4TG144C	7000-LUT device packaged in a 20 x 20mm, 144-pin TQFP
Interfaces			
LED Array	Output	D8-D1	Red LEDs
Four 2 × 20 Header Landings	I/O	J2: header_2x20 J3: header_2x20 J4: header_2x20 J5: header_2x20	User-definable I/O
1 × 8 Header Landing	I/O	J1: header_1x8	Optional JTAG interface
4 × 15 60-Hole Prototype Area	—	—	Prototype area 100mil centered holes.
Test Points	Power	TP1: +3.3 V TP2: +1.2 V TP3: GND	Power and ground reference points

7.2. Subsystems

This section describes the principle subsystems for the Breakout Board in alphabetical order.

7.2.1. Clock Sources

All clocks for the counter demonstration designs originate from the MachXO2 on-chip oscillator. You may use an expansion header landing to drive a FPGA input with an external clock source.

7.2.2. Expansion Header Landings

The expansion header landings provide access to user GPIOs, primary inputs, clocks, and VCCO pins of the MachXO2. The remaining pins serve as power supplies for external connections. Each landing is configured as one 2 x 20 100 mil.

Table 7.2. Expansion Connector Reference

Item	Description
Reference Designators	J2, J3, J4, J5
Part Number	header_2x20

Table 7.3. Expansion Header Pin Information (J2)

Header Pin Number	-1200ZE Function	-7000HE Function	MachXO2 Pin
1	NC	NC	—
2	VCCIO0	VCCIO0	118, 123, 135
3	PT17D / DONE	PT36D / DONE	109
4	PT17C / INITn	PT36C / INITn	110
5	PT17B	PT36B	111
6	PT17A	PT36A	112
7	GND	GND	—
8	GND	GND	—
9	PT16D	PT33B	113
10	PT16C	PT33A	114
11	PT16B	PT28B	115
12	PT16A	PT28A	117
13	PT15D / PROGn	PT27D / PROGn	119
14	PT15C / JTAGen	PT27C / JTAGen	120
15	GND	GND	—
16	GND	GND	—
17	PT15B	PT25B	121
18	PT15A	PT25A	122
19	PT12D / SDA / PCLKC0_0	PT22D / SDA / PCLKC0_0	125
20	PT12C / SCL / PCLKT0_0	PT22C / SCL / PCLKT0_0	126
21	PT12B / PCLKC0_1	PT18B / PCLKC0_1	127
22	PT12A / PCLKT0_1	PT18A / PCLKT0_1	128
23	GND	GND	—
24	GND	GND	—
25	PT11D / TMS	PT17D / TMS	130
26	PT11C / TCK	PT17C / TCK	131
27	PT11B	PT15B	132
28	PT11A	PT15A	133
29	PT10D / TDI	PT14D / TDI	136
30	PT10C / TDO	PT14C / TDO	137
31	GND	GND	—
32	GND	GND	—
33	PT10B	PT11B	138
34	PT10A	PT11A	139
35	PT9D	PT10B	140
36	PT9C	PT10A	141
37	PT9B	PT9B	142
38	PT9A	PT9A	143
39	GND	GND	—
40	GND	GND	—

Table 7.4. Expansion Header Pin Information (J3)

Header Pin Number	-1200ZE Function	-7000HE Function	MachXO2 Pin
1	VCC_1.2V	VCC_1.2V	36, 72, 108, 144
2	VCCIO1	VCCIO1	79, 88, 102
3	VCC_1.2V	VCC_1.2V	36, 72, 108, 144
4	NC	NC	—
5	PR10C	PR24A	74
6	PR10D	PR24B	73
7	PR10A	PR23A	76
8	PR10B	PR23B	75
9	GND	GND	—
10	GND	GND	—
11	PR9C	PR21A	78
12	PR9D	PR21B	77
13	PR9A	PR18A	82
14	PR9B	PR18B	81
15	GND	GND	—
16	GND	GND	—
17	PR8C	PR17A	84
18	PR8D	PR17B	83
19	PR8A	PR16A	86
20	PR8B	PR16B	85
21	GND	GND	—
22	GND	GND	—
23	PR5C / PCLKT1_0	PR12A / PCLKT1_0	92
24	PR5D / PCLKC1_0	PR12B / PCLKC1_0	91
25	PR5A	PR11A	94
26	PR5B	PR11B	93
27	GND	GND	—
28	GND	GND	—
29	PR4C	PR9A	96
30	PR4D	PR9B	95
31	PR4A	PR7A	98
32	PR4B	PR7B	97
33	GND	GND	—
34	GND	GND	—
35	PR3A	PR5A	100
36	PR3B	PR5B	99
37	PR2C	PR3A	105
38	PR2D	PR3B	104
39	PR2A	PR2A	107
40	PR2B	PR2B	106

Table 7.5. Expansion Header Pin Information (J4)

Header Pin Number	-1200ZE Function	-7000HE Function	MachXO2 Pin
1	VCC_3.3V	VCC_3.3V	—
2	VCCIO3	VCCIO3/4/5	30(VCCIO3), 16(VCCIO4), 7(VCCIO5)
3	VCC_3.3V	VCC_3.3V	—
4	NC	NC	—
5	PL2A / L_GPLLT_FB	PL3A / L_GPLLT_FB	1
6	PL2B / L_GPPLC_FB	PL3B / L_GPPLC_FB	2
7	PL2C / L_GPLLT_IN	PL4A / L_GPLLT_IN	3
8	PL2D / L_GPLLC_IN	PL4B / L_GPLLC_IN	4
9	PL3A / PCLKT3_2	PL6A / PCLKT5_0	5
10	PL3B / PCLKC3_2	PL6B / PCLKC5_0	6
11	PL3C	PL8A	9
12	PL3D	PL8B	10
13	GND	GND	—
14	GND	GND	—
15	PL4A	PL9A	11
16	PL4B	PL9B	12
17	PL4C	PL10A	13
18	PL4D	PL10B	14
19	GND	GND	—
20	GND	GND	—
21	PL5A / PCLKT3_1	PL12A / PCLKT4_0	19
22	PL5B / PCLKC3_1	PL12B / PCLKC4_0	20
23	PL5C	PL15A	21
24	PL5D	PL15B	22
25	GND	GND	—
26	GND	GND	—
27	PL8A	PL17A	23
28	PL8B	PL17B	24
29	PL8C	PL19A	25
30	PL8D	PL19B	26
31	GND	GND	—
32	GND	GND	—
33	PL9A / PCLKT3_0	PL22A / PCLKT3_0	27
34	PL9B / PCLKC3_0	PL22B / PCLKC3_0	28
35	GND	GND	—
36	GND	GND	—
37	PL10A	PL24A	32
38	PL10B	PL24B	33
39	PL10C	PL25A	34
40	PL10D	PL25B	35

Expansion Header Pin Information (J5)

Header Pin Number	-1200ZE Function	-7000HE Function	MachXO2 Pin
1	NC	NC	—
2	VCCIO2	VCCIO2	37, 51, 66
3	PB20D / SI / SISPI	PB38B / SI / SISPI	71
4	PB20B	PB37B	69
5	PB20C / SN	PB38A / SN	70
6	PB20A	PB37A	68
7	PB18D	PB35B	67
8	PB18B	PB31B	62
9	PB18C	PB35A	65
10	PB18A	PB31A	61
11	GND	GND	—
12	GND	GND	—
13	PB15D	PB29B	60
14	PB15B	PB26B	58
15	PB15C	PB29A	59
16	PB15A	PB26A	57
17	GND	GND	—
18	GND	GND	—
19	PB11B / PCLKC2_1	PB23B / PCLKC2_1	56
20	PB11D	PB18B	54
21	PB11A / PCLKT2_1	PB23A / PCLKT2_1	55
22	PB11C	PB18A	52
23	GND	GND	—
24	GND	GND	—
25	PB9B / PCLKC2_0	PB16B / PCLKC2_0	50
26	PB9D	PB13B	48
27	PB9A / PCLKT2_0	PB16A / PCLKT2_0	49
28	PB9C	PB13A	47
29	GND	GND	—
30	GND	GND	—
31	PB6D / SO / SPISO	PB12B / SO / SPISO	45
32	PB6B	PB9B	43
33	PB6C / MCLK / CCLK	PB12A / MCLK / CCLK	44
34	PB6A	PB9A	42
35	GND	GND	—
36	GND	GND	—
37	PB4D	PB6B	41
38	PB4B	PB4B	39
39	PB4C / CSSPIN	PB6A / CSSPIN	40
40	PB4A	PB4A	38

J2

1	2
NC	IO0
109	110
111	112
GND	GND
113	114
115	117
119	120
GND	GND
121	122
125	126
127	128
GND	GND
130	131
132	133
136	137
GND	GND
138	139
140	141
142	143
GND	GND

J4

1	2
3.3	IO3
3.3	NC
1	2
3	4
5	6
9	10
GND	GND
11	12
13	14
GND	GND
19	20
21	22
GND	GND
23	24
25	26
GND	GND
27	28
GND	GND
32	33
34	35

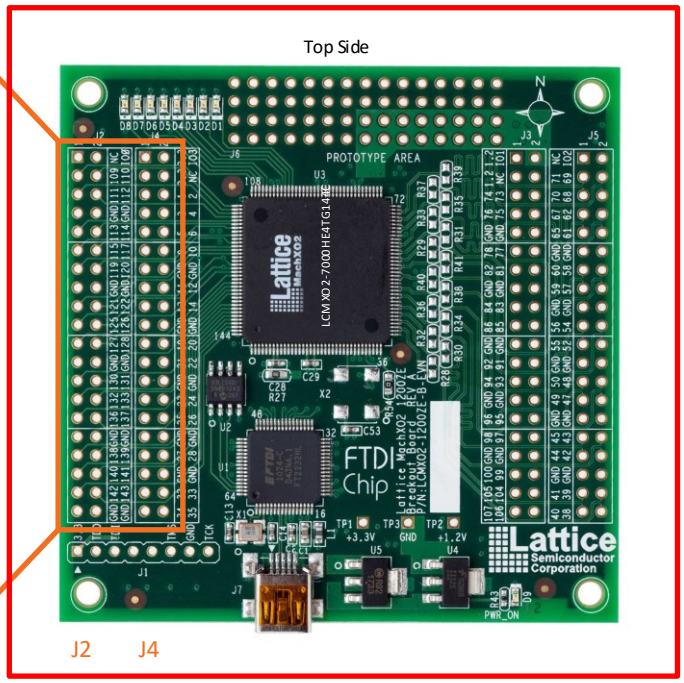
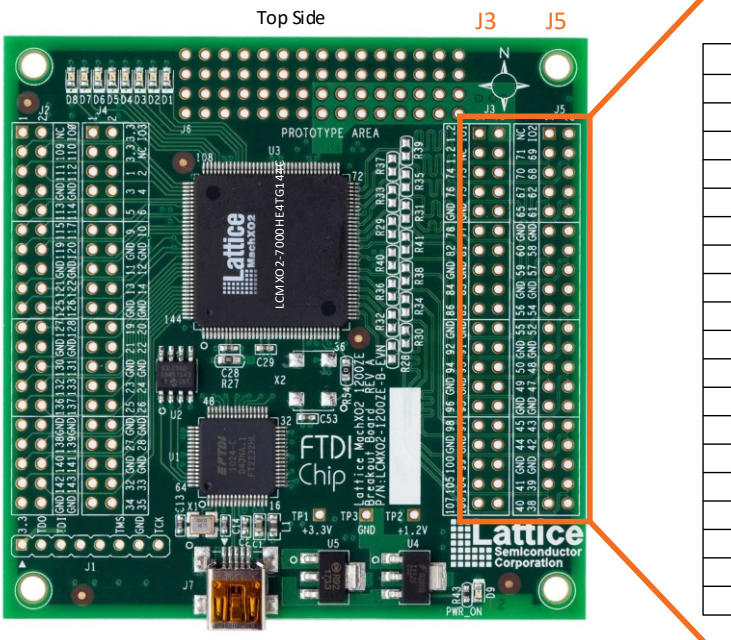


Figure 7.2. J3/J4 Header Landing Callout



J3

1	2
1.2	IO1
1.2	NC
74	73
76	75
GND	GND
78	77
82	81
GND	GND
84	83
86	85
GND	GND
92	91
94	93
GND	GND
96	95
98	97
GND	GND
100	99
105	104
107	106

J5

1	2
NC	IO2
71	69
70	68
67	62
65	61
GND	GND
60	58
59	57
GND	GND
56	54
55	52
GND	GND
50	48
49	47
GND	GND
45	43
44	42
GND	GND
41	39
40	38

Figure 7.3. J3/J5 Header Landing Callout

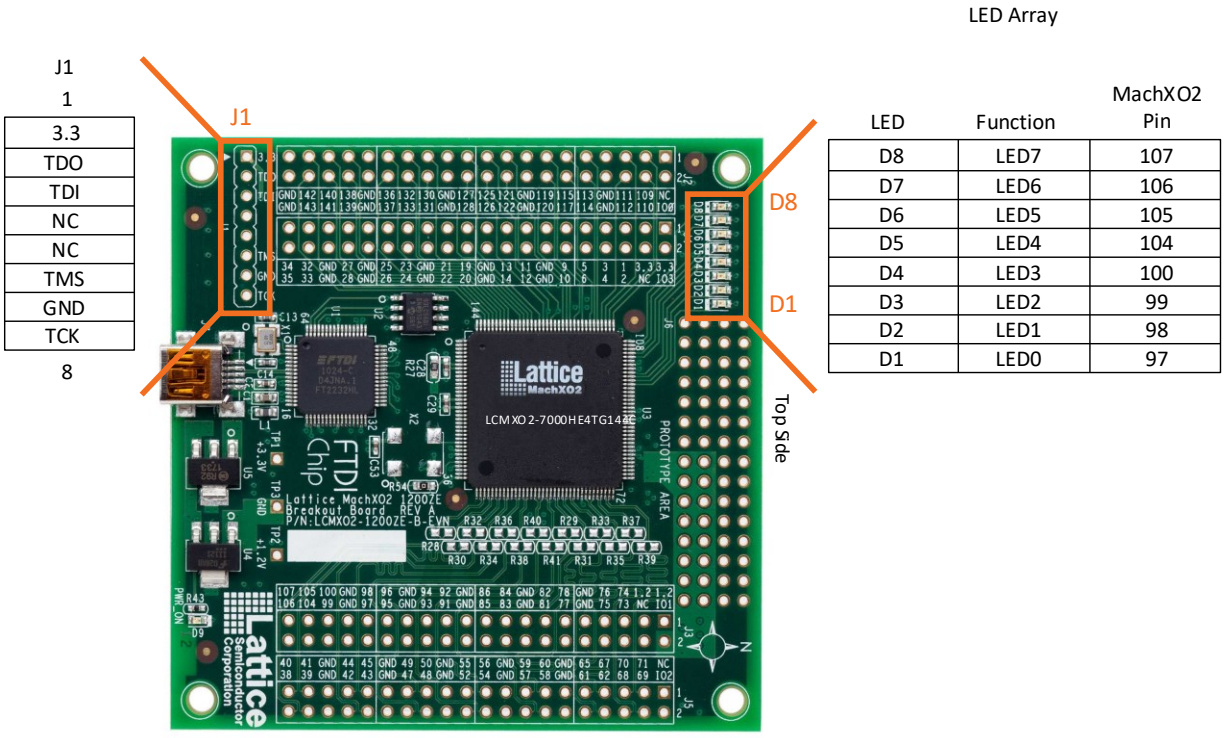


Figure 7.4. J1 Header Landing and LED Array Callout

7.2.3. MachXO2 FPGA

The MachXO2-7000HE-4TG144C is a 144-pin TQFP package FPGA device which provides up to 114 usable I/O in a 20 mm × 20 mm package. 108 I/O are accessible from the breakout board headers.

Table 7.6. MachXO2 and MachXO3 FPGA Interface Reference

Item	Description
Reference Designators	U3
Part Number	LCMXO2-7000HE-4TG144C
Manufacturer	Lattice Semiconductor
Web Site	www.latticesemi.com

7.2.4. JTAG Interface Circuits

For power and programming an FTDI USB UART/FIFO IC converter provides a communication interface between a PC host and the JTAG programming chain of the Breakout Board. The USB 5V supply is also used as a source for the 3.3 V supply rail. A USB mini-B socket is provided for the USB connector cable.

Table 7.7. JTAG Interface Reference

Item	Description
Reference Designators	U1
Part Number	FT2232HL
Manufacturer	Future Technology Devices International (FTDI)
Web Site	www.ftdichip.com

Table 7.8. JTAG Programming Pin Informationz

Description	MachXO2 Pin
Test Data Output	137:TDO
Test Data Input	136:TDI
Test Mode Select	130:TMS
Test Clock	131:TCK

Table 7.9. LEDs

A green LED (D9) is used to indicate USB 5V power. Eight red LEDs are driven by I/O pins of the MachXO2 device.

Table 7.10. Power and User LEDs Reference

Item	Description
Reference Designators	Red LEDs (D1, D2, D3, D4, D5, D6, D7, D8) Green LEDs (D9)
Part Number	LTST-C190KRKT (D1-D8) LTST-C190KGKT (D9)
Manufacturer	Lite-On It Corporation
Web Site	www.liteonit.com

7.2.5. Power Supply

3.3 V and 1.2 V power supply rails are converted from the USB 5 V interface when the board is connected to a host PC.

7.2.6. Test Points

In order to check the various voltage levels used, the following test points are provided:

- TP1: +3.3 V
- TP2: +1.2 V
- TP3: GND

7.2.7. USB Programming and Debug Interface

The USB mini-B socket of the Breakout Board serves as the programming and debug interface.

JTAG Programming: For JTAG programming, a preprogrammed USB PHY peripheral controller is provided on the Breakout Board to serve as the programming interface to the MachXO2 FPGA.

Programming requires the Lattice Diamond or ispVM System software.

Table 7.11. USB Interface Reference

Item	Description
Reference Designators	U1
Part Number	FT2232HL
Manufacturer	Future Technology Devices International (FTDI)
Web Site	www.ftdichip.com

7.3. Board Modifications

This section describes modifications to the board to change or add functionality.

7.3.1. Bypassing the USB Programming Interface

The USB programming interface circuit (USB Programming and Debug Interface section) may be optionally by-passed by removing the 0 ohm resistors: R5, R6, R7, R8 (See Appendix A. Schematic Diagram, Sheet 2 of 5). Header landing J1 provides JTAG signal access for jumper wires or a 1 × 8 pin header.

7.3.2. Applying External Power

The Breakout Board is powered by the circuit of Schematic Sheet 5 of 5 based on the 5 V USB power source. You may disconnect this power source by removing the 0 Ω resistors: R42 (VCC_1.2 V) and R44 (VCC_3.3 V). Power connections are available from the expansion header landings, J3 (+1.2 V, pins 1 and 3, schematic sheet 3 of 5) and J4 (+3.3 V, pins 1 and 3, schematic sheet 4 of 5).

7.3.3. Measuring Bank and Core Power

In addition to the expansion headers, test points (TP1, TP2) provide access to power supplies of the MachXO2 FPGA. Inline 1 ohm resistors: R24 (VCCIO0, +3.3 V, Bank 0), R25 (VCCIO1, +3.3 V, Bank 1), R26 (VCCIO2, +3.3 V, Bank 2), R27 (VCCIO3, +3.3 V, Bank 3), R56 (VCC core, +1.2 V) can be used to measure current for the power supplies. VCCIO3 (Bank 3), VCCIO4 (Bank 4) and VCCIO5 (Bank 5) in the current version of the board with LCMXO2-7000HE-4TG144C device are all connected to the same +3.3V supply.

7.4. Mechanical Specifications

Dimensions: 3 in. [L] × 3 in. [W] × 1/2 in. [H]

7.5. Environmental Requirements

The evaluation board must be stored between -40° C and 100° C. The recommended operating temperature is between 0° C and 90° C.

The board can be damaged without proper anti-static handling.

7.6. Glossary

FPGA — Field Programmable Gate Array

DIP — Dual in-line package

LED — Light Emitting Diode.

LUT — Look Up Table

PCB — Printed Circuit Board

RoHS — Restriction of Hazardous Substances Directive

USB — Universal Serial Bus

WDT — Watchdog Timer

8. Troubleshooting

Use the tips in this section to diagnose problems with the Breakout Board.

8.1. LEDs Do Not Flash

If power is applied but the board does not flash according to the preprogrammed counter demonstration, then it is likely the board has been reprogrammed with a new design. Follow the directions in the Demonstration Design section to restore the factory default.

8.2. USB Cable Not Detected

If Lattice Diamond Programmer or ispVM System does not recognize the USB cable after installing the Lattice USB port drivers and rebooting, the incorrect USB driver may have been installed. This usually occurs if you attach the board to your PC prior to installing the Lattice-supplied USB driver.

8.3. To access the Troubleshooting the USB Driver Installation Guide

To access the installation guide for Diamond software and standalone Diamond Programmer:

1. Start Diamond or Diamond Programmer and choose **Help**.
2. Search for **USB driver** or **Troubleshooting**, then select the **Troubleshooting the USB Driver** topic.
3. Follow the directions to install the Lattice USB driver.

To access the installation guide for ispVM:

1. Start ispVM System and choose **Options > Cable and I/O Port Setup**. The Cable and I/O Port Setup Dialog appears.
2. Click the **Troubleshooting the USB Driver Installation Guide** link. The Troubleshooting the USB Driver Installation Guide document appears in your system's PDF file reader.
3. Follow the directions to install the Lattice USB driver.

8.4. Determine the Source of a Pre-Programmed Device

If the Breakout Board has been reprogrammed, the original demo design can be restored. To restore the board to the factory default, see the Download Demo Designs section for details on downloading and reprogramming the device.

9. Ordering Information

Table 9.1. Ordering Information

Description	Ordering Part Number	China RoHS Environment-Friendly Use Period (EFUP)
MachXO2-7000HE Breakout Board Evaluation Kit	LCMXO2-7000HE-B-EVN	
MachXO2 Breakout Board Evaluation Kit	LCMXO2-1200ZE-B-EVN*	

***Note**: For reference only. This version of the board is no longer available for sale.

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Appendix A. Schematic Diagrams

Note: The schematics are drawn using the MachXO2-1200ZE device. Please consult Tables 3 through 6 for -1200 and -7000HE pin name and bank synonyms. Pin numbers are correct for either device.

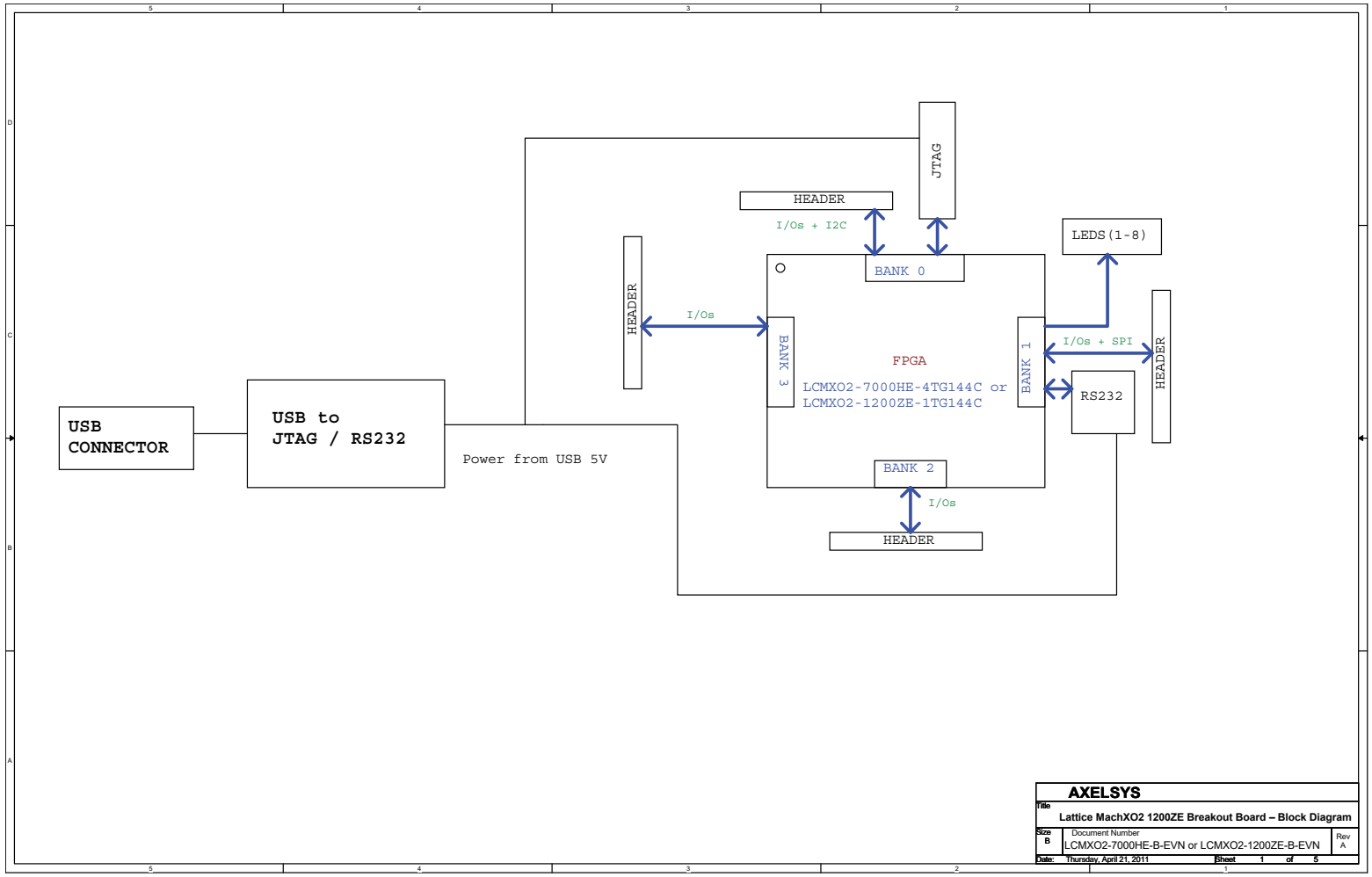


Figure A.1. Block Diagram

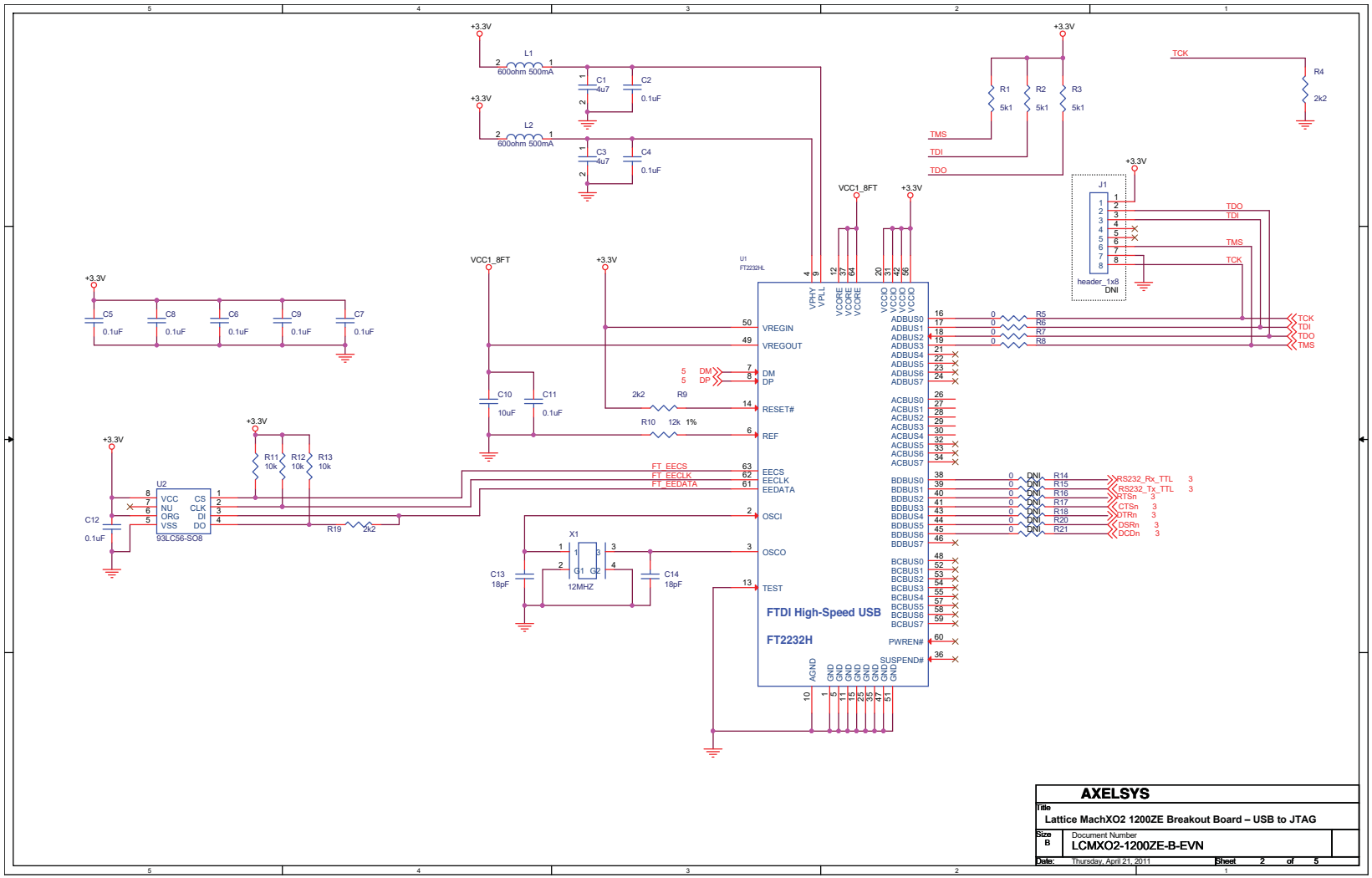


Figure A.2. USB Interface to JTAG

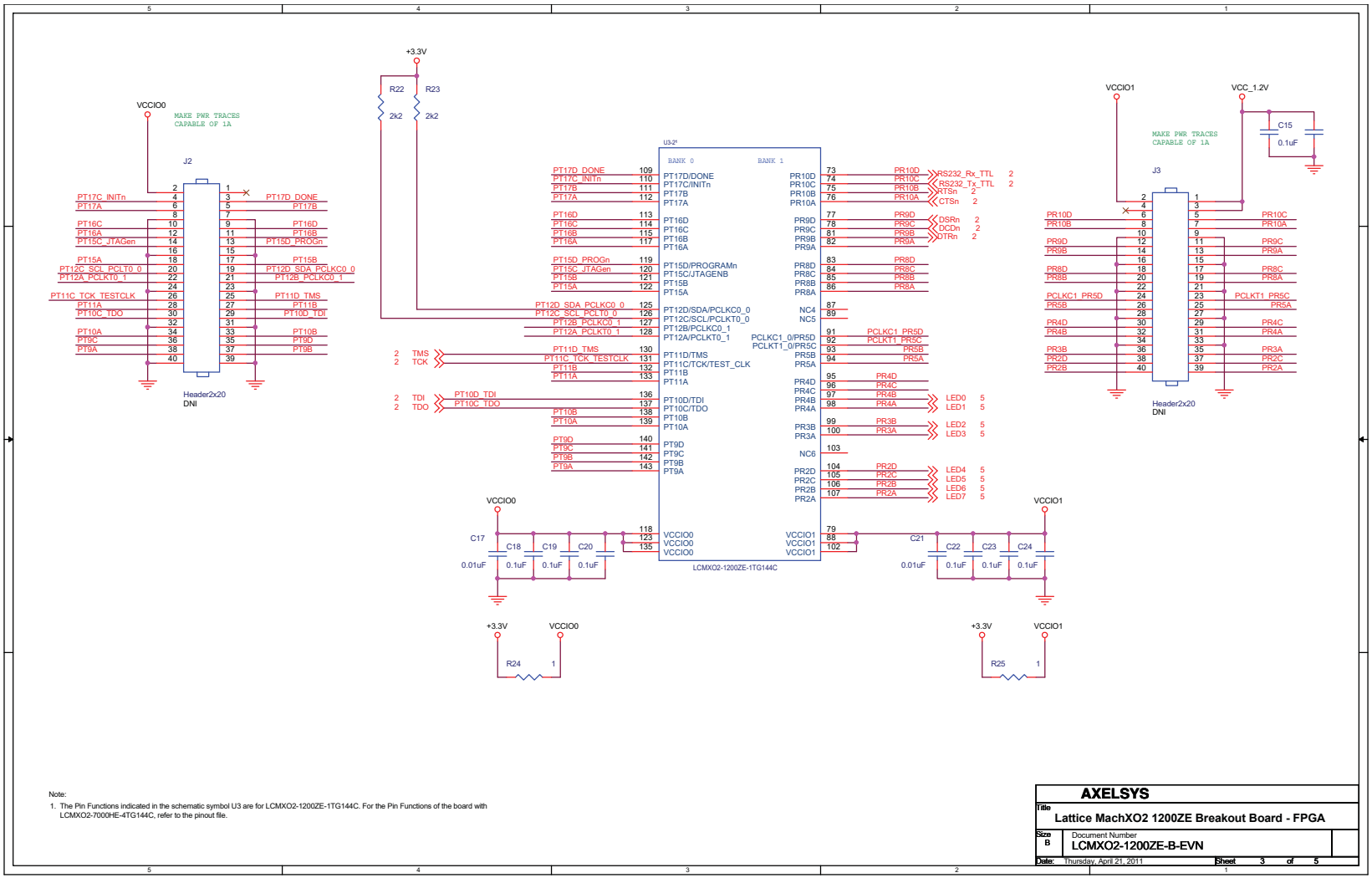


Figure A.3. FPGA

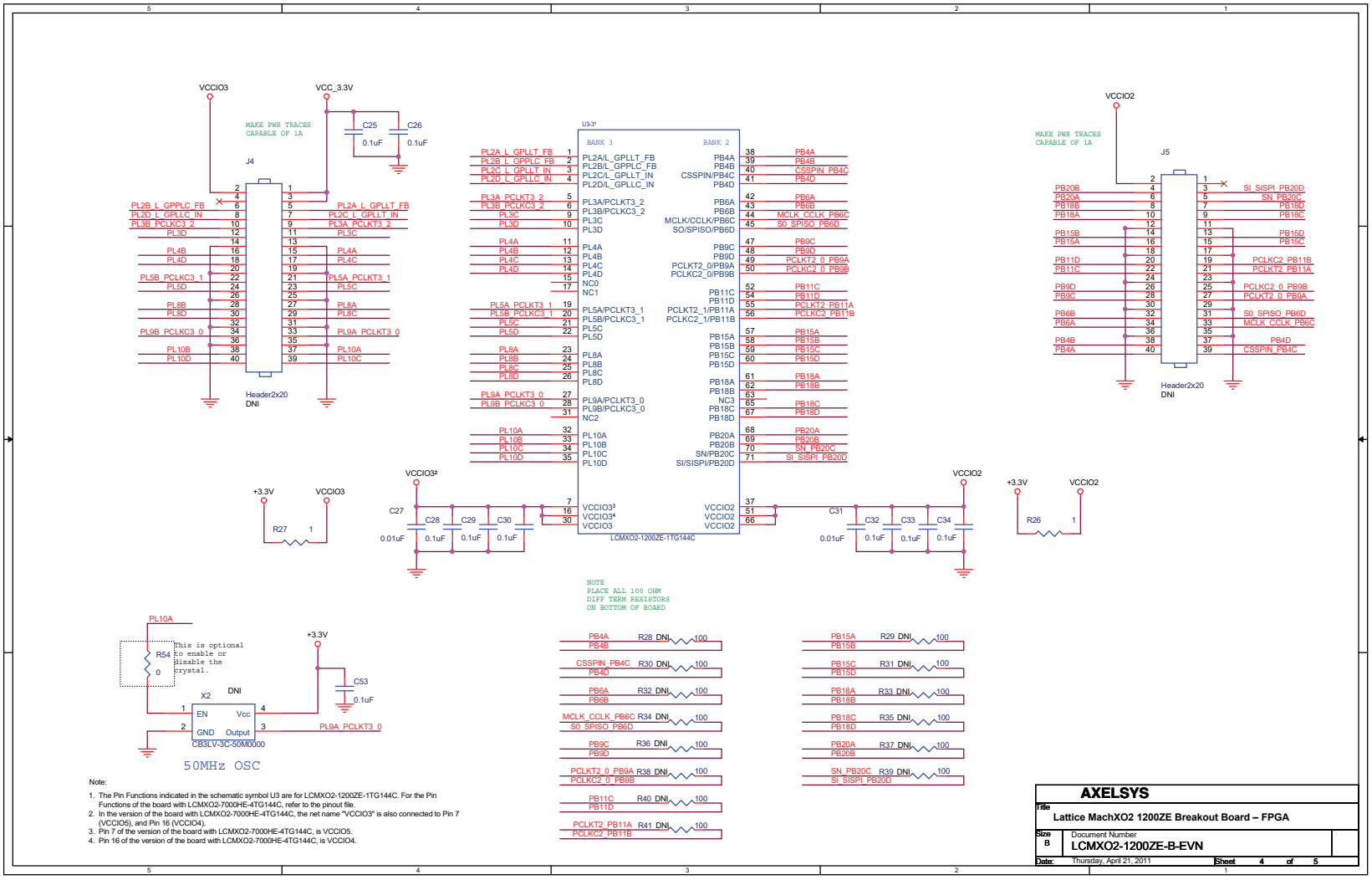


Figure A.4. FPGA

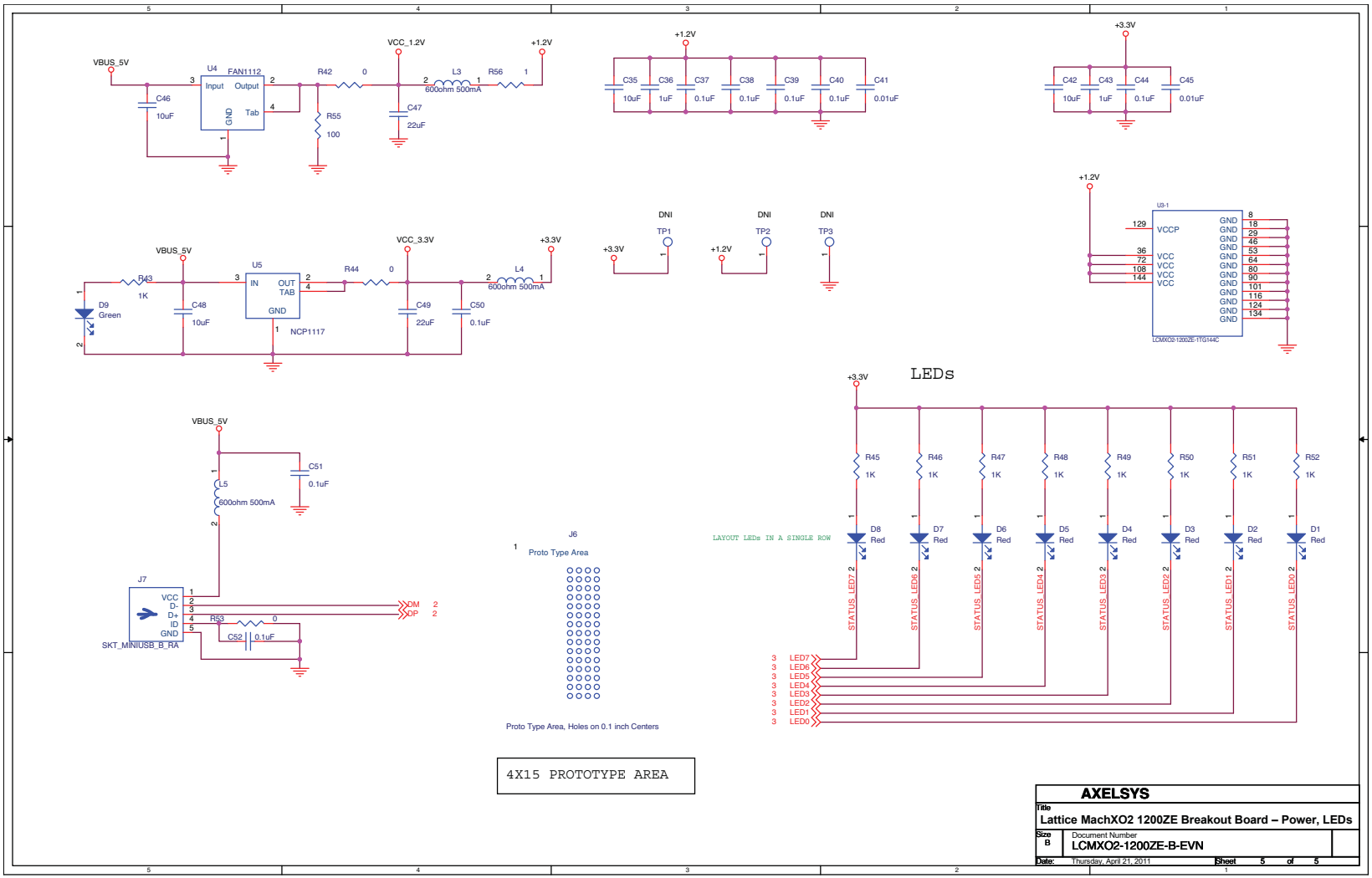


Figure A.5. Power LEDs

Appendix B. Bill of Materials

Item	Quantity	Reference	Value	Manufacturer	MFG Pin
Item	Quantity	Reference	Manufacturer	Item	Quantity
1	2	C1, C3	Panasonic	1	2
2	34	C2, C4, C5, C6, C7, C8, C9, C11, C12, C15, C16, C18, C19, C20, C22, C23, C24, C25, C26, C28, C29, C30, C32, C33, C34, C37, C38, C39, C40, C44, C50, C51, C52, C53	Kemet	2	34
3	5	C10, C35, C42, C46, C48	Taiyo Yuden	3	5
4	2	C13, C14	Kemet	4	2
5	6	C17, C21, C27, C31, C41, C45	Kemet	5	6
6	2	C36, C43	Kemet	6	2
7	2	C47, C49	Taiyo Yuden	7	2
8	8	D1, D2, D3, D4, D5, D6, D7, D8	LITE-On, Inc.	8	8
9	1	D9	LITE-On, Inc.	9	1
10	1	J1	Molex	10	1
11	4	J2, J3, J4, J5	Samtec	11	4
12	1	J6		12	1
13	1	J7	Neltron	13	1
14	5	L1, L2, L3, L4, L5	Murata	14	5
15	3	R1, R2, R3	Yageo	15	3
16	5	R4, R9, R19, R22, R23	Yageo	16	5
17	8	R5, R6, R7, R8, R42, R44, R53, R54	Yageo	17	8
18	1	R10	Yageo	18	1
19	3	R11, R12, R13	Yageo	19	3
20	7	R14, R15, R16, R17, R18, R20, R21	Yageo	20	7
21	5	R24, R25, R26, R27, R56	Vishay/Dale	21	5
22	14	R28, R29, R30, R31, R32, R33, R34, R35, R36, R37, R38, R39, R40, R41	Yageo	22	14
23	9	R43, R45, R46, R47, R48, R49, R50, R51, R52	Yageo	23	9
24	1	R55	Yageo	24	1
25	3	TP1, TP2, TP3		25	3
26	1	U1	FTDI	26	1
27	1	U2	Microchip	27	1
28	1	U3	Lattice	28	1

Item	Quantity	Reference	Value	Manufacturer	MFG Pin
29	1	U4	Fairchild Semi	29	1
30	1	U5	On Semi	30	1
31	1	X1	TXC	7M-12.000MAAJ-T	31
32	1	X2	CTS	CB3LV-3C-50M0000	32

Revision History

Revision 2.3, February 2022

Section	Change Summary
MachXO2 Breakout Board	• Changed “30, 16, 7” to “30(VCCIO3), 16(VCCIO4), 7(VCCIO5)” in the MachXO2 Pin column for header pin number 2 in Table 7.5. Expansion Header Pin Information (J4). • Added a rectangle around Figure 7.2. J3/J4 Header Landing Callout. • Added “VCCIO3 (Bank 3), VCCIO4 (Bank 4) and VCCIO5 (Bank 5) in the current version of the board with LCMXO2-7000HE-4TG144C device are all connected to the same +3.3V supply.” to Section 7.3.3. Measuring Bank and Core Power.
Appendix A. Schematic Diagrams	• Added footnote 1 and removed “LCMXO2-7000HE-4TG144C” from Figure A.3. FPGA. • Added footnote 1, 2, 3 and 4 and removed “LCMXO2-7000HE-4TG144C” from Figure A.4. FPGA.

Revision 2.2, January 2014

Section	Change Summary
All	Updated description and procedure for downloading demo designs in Download Demo Designs section.
	Updated project file name in Programming a Demo Design with the Lattice Diamond Programmer section.

Revision 2.1, September 2013

Section	Change Summary
All	Updated procedure in Programming a Demo Design with the Lattice Diamond Programmer section.
	Added information to the procedure on loading the FTDI chip USB hardware drivers via the standalone package:
	Updated description of Reference Designators in the Power and User LEDs Reference table.

Revision 2.0, February 2013

Section	Change Summary
All	Updated Tables 3-6 to include -7000HE information. Added -7000HE notes to Figure 3 and Appendix A.

Revision 1.2, December 2012

Section	Change Summary
All	Updated document to describe new version of the board featuring the MachXO2-7000HE. Indicated that the MachXO2-1200ZE version of the board is no longer available.

Revision 1.1, January 2012

Section	Change Summary
Features	MachXO2-1200ZE Breakout Board, Top Side figure updated with revision B board photo.

Revision 1.0, December 2011

Section	Change Summary
All	Initial release.

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